REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants have amended each of independent claims 2 and 13 to recite, in step (c), that the wafer is transferred to a post cleaning section while keeping "a surface of the metal layer left in the wiring groove pattern" (or "a surface of the metal layer left in the first and second wiring groove patterns") of the major surface of the wafer wet with moving water. Note, for example, Figs. 8 and 12 and descriptions on pages 26-30, of Applicants' disclosure. Claims 5, 6, 10, 16, 17, 20 and 21 have been amended in light of amendments to claims 2 and 13.

In addition, Applicants are adding claims 22 and 23 to the application. Claims 22 and 23 are dependent respectively on claims 2 and 13, and each recite that the chemical mechanical polishing uses an abrasive grain-free procedure.

The obviousness-type double patenting rejection set forth in Item 4 on page 5 of the Office Action mailed April 22, 2005, is noted. Submitted herewith is a Terminal Disclaimer in the above-identified application, with respect to U.S. Patent No. 6,531,400. It is respectfully submitted that this Terminal Disclaimer satisfies all applicable requirements of 37 CFR 1.321(c). In view of the filing of this Terminal Disclaimer, it is respectfully submitted that the obviousness-type double patenting rejection is moot.

The enclosed Terminal Disclaimer is being presently submitted in order to facilitate proceedings in connection with the above-identified application, so as to achieved earliest possible issuance of a U.S. patent based thereon. It is respectfully submitted that the filing of this Terminal Disclaimer does not constitute an admission as to the propriety of, or agreement with, the obviousness-type double patenting

rejection; and does not constitute an admission as to the propriety, or agreement with, arguments made by the Examiner in connection with the obviousness-type double patenting rejection.

Applicants respectfully submit that all of the claims presented for consideration by the Examiner patentably distinguish over the teachings of the references applied by the Examiner in rejecting claims in the Office Action mailed April 22, 2005, that is, the teachings of U.S. Patent No. 6,153,043 to Edelstein, et al., and Japanese Patent Document No. 07-135192 (hereinafter referred to as referred to by the Examiner, i.e., "Hideaki"), under the provisions of 35 USC 103.

It is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a process for manufacturing a semiconductor integrated circuit device as in the present claims, having the steps as in the present claims, including, in particular, wherein after the metal layer is removed outside the wiring groove pattern by a chemical mechanical polishing method so as to leave the metal layer in the wiring groove pattern, the wafer is transferred to a post cleaning section of single wafer processing apparatus, while keeping the surface of the metal layer left in the wiring groove pattern wet with moving water, with scrub or brush cleaning thereafter being performed to the first major surface of the wafer with a liquid chemical or pure water in the post cleaning section. See claim 2.

In addition, it is respectfully submitted that these applied references would have neither disclosed nor would have suggested such method, including wherein the metal layer outside first and second wiring groove patterns is removed by a chemical mechanical polishing section of a single wafer processing apparatus, with the wafer thereafter being transferred to a post cleaning section of the single wafer

processing apparatus while keeping the surface of the metal layer left in the first and second wiring groove patterns of the first major surface of the wafer wet with moving water, with the above-referred-to scrub or brush cleaning being performed in the post cleaning section. See claim 13.

Furthermore, it is respectfully submitted that these applied references would have neither disclosed nor would have suggested such process as in the present claims, having features as discussed previously in connection with claims 2 and 13, and, moreover, wherein the moving water is a water shower (see, e.g., claims 3, 7, 14 and 18); and/or wherein the metal layer left in the wiring groove pattern, or first and second wiring groove patterns, constitutes a portion of a metal wiring of a dual damasene wiring (see, e.g., claims 4, 9, 15 and 19); and/or wherein the scrub or brush cleaning is performed prior to a substantial progress of corrosion of a surface of the metal layer left in the wiring groove pattern or patterns (see, e.g., claims 5, 16 and 20); and/or wherein the surface of the metal layer left in the wiring groove pattern or patterns is kept wet from the end of the removal of the metal layer by chemical mechanical polishing to the scrub or brush cleaning (see claims 6, 10, 17 and 21), and/or wherein the light shielding structure includes a light shielding sheet (see claims 11 and 12).

The present invention is directed to a technique for manufacturing a semiconductor integrated circuit device, effective in achieving anticorrosion of metal wirings formed by a chemical mechanical polishing (CMP).

As described on page 1 of Applicants' specification, the secondary reference as applied by the Examiner in the Office Action mailed April 22, 2005, referred to in the Office Action as Hideaki, discloses a post-polishing method which makes it possible to lower the particle level after polishing treatment on the wafer, by

performing, without drying the wafer, a series of steps including a wet state for the wafer. As described in the reference, the wafer is kept wet for reducing siloxane linkage on the surface of a SiO_2 insulating film. That is, this reference discloses that a silica particle used in chemical mechanical polishing tends to combine by a hydrogen linkage to an SiO_2 film when the wafer is in a condition of a dry wafer. This linkage is hard to break, and thus it is hard to remove the silica particle. Hideaki discloses that the wafer should be kept wet during transfer from chemical mechanical polishing to the cleaning section, for preventing linkage of the SiO_2 insulating film with the silica particles. Note, for example, page 1, lines 14-24, of Applicants' specification. See the enclosed copy of U.S. Patent No. 5,779,520, issued July 14, 1998, which is a patent family member of Hideaki.

As described on page 2 of the Applicants' specification (for example, page 2, lines 19-22), a metal chemical mechanical polishing process using a slurry containing an anticorrosive agent has been described, so as to prevent corrosion of the metal which might otherwise occur in the metal chemical mechanical polishing process.

However, notwithstanding the foregoing, it is still desired to provide a simplified process for that avoids corrosion of the metal after chemical mechanical polishing thereof. The desirability of a process avoiding corrosion of the metal due to chemical mechanical polishing thereof has become particularly acute in recent years, as the integration of large scale integrated circuits has increased, and where attention has been given to wirings using copper. Specifically, when the copper film is polished by a chemical mechanical polishing method, a portion of the copper may be eluted by the action of an oxidizing agent added to the polishing slurry, so that a

portion of the copper wiring is corroded, thereby bringing about open defects or short-circuit defects.

Against this background, Applicants provide a process avoiding such corrosion of copper wirings, avoiding the above-referred-to open defects or short-circuit defects. Applicants have found that, in using a single wafer processing apparatus, by utilizing a light-shielding structure enclosing the post cleaning section and between the chemical mechanical polishing section and the post cleaning section; and also by transferring the wafer after the chemical mechanical polishing to a post cleaning section of the single wafer processing apparatus while keeping the surface of the metal layer left in the wiring groove pattern of the first major surface of the wafer wet with moving water, corrosion of the metal layer in the wiring groove pattern (for example, copper, e.g., deposited by electrolytic deposition) can be avoided.

It is emphasized that according to the present invention, the surface of the metal layer left in the wiring groove pattern or patterns is kept wet after removal of the metal layer outside the wiring groove pattern or patterns by chemical mechanical polishing, so as to avoid corrosion of the metal layer. In contrast, Hideaki discloses that wetting of the wafers prevents the formation of covalent bonding between silica particles which are polishing abrasive grains and the surface of the SiO_2 insulating film. It is respectfully submitted that this reference does not disclose, nor would have suggested, the process as in the present claims, including wherein after removing the metal layer outside the wiring groove pattern by a chemical mechanical polishing method, the wafer is transferred to a post cleaning section of the single wafer processing apparatus, while keeping the surface of the metal layer in the groove wet with moving water, and advantages thereof.

Edelstein, et al. discloses a method for eliminating dissolution and/or corrosion of metallic conductors induced by light exposure of partially fabricated semiconductor devices, the method utilizing a darkened enclosure, such as a box or curtains, for use on tools for wafer chemical mechanical polishing, brush cleaning, unloading and rinsing. This patent also discloses that, alternatively, illumination of the wafer can be limited to wavelengths of light that do not provide enough energy to promote any electrons in the PN junctions from the valence band to the conduction band. See column 2, lines 8-14. Note also the paragraph bridging columns 1 and 2 of this patent. Note, further, column 2, lines 17-21, disclosing use of an inhibitor in the polishing slurry or post chemical mechanical water rinse, to prevent an electrochemical dissolution reaction. Note also column 6, lines 34-41. See also column 7, lines 19-52.

It is respectfully submitted that Edelstein, et al. would have neither taught nor would have suggested such process as in the present claims, including use of both the light shielding structure, in a single wafer processing apparatus, enclosing the post cleaning section and between the chemical mechanical polishing section and the post cleaning section, together with the transfer of the wafer to the post cleaning section of the single wafer processing apparatus, after the chemical mechanical polishing, while keeping the surface of the metal layer left in the wiring groove pattern wet with moving water.

It is respectfully submitted that the additional teachings of Hideaki would not have rectified the deficiencies of Edelstein, et al., such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art. Hideaki has been previously discussed herein; and attention is again directed to the enclosed U.S. Patent No. 5,779,520, which is a family patent of Hideaki. It is again

emphasized that Hideaki is directed to keeping a SiO_2 insulating film surface wet for preventing this surface from hydrogen linkage with silica particles. It is respectfully submitted that the disclosure of this Japanese patent document would have neither taught nor would have suggested, either alone or in combination with the teachings of Edelstein, et al., keeping the surface of the metal layer left in the wiring groove pattern wet with moving water, and advantages thereof including, for example, avoiding corrosion thereof.

Note especially that Hideaki has a purpose of avoiding hydrogen linkage of abrasive grains of the polishing slurry with the insulating. The disclosure of this patent document, together with the teachings of Edelstein, et al., would have especially taught away from the abrasive grain-free polishing procedure as in claims 22 and 23.

The contention by the Examiner on page 3 of the Office Action mailed April 22, 2005, that Hideaki discloses the use of wet wafer transfer, is noted. It is emphasized, however, as discussed previously, that Hideaki discloses, e.g., wherein the formation of covalent bonding between silica particles, which are polishing abrasive grains, and the surface of an SiO_2 film, is prevented by wetting of the wafers. It is respectfully submitted that this reference would not have disclosed nor would have suggested, either alone or in combination with the teachings of Edelstein, et al., keeping the surface of the metal layer left in the wiring groove pattern or patterns wet with moving water, in transferring the wafer to the post cleaning section of the single wafer processing apparatus.

In view of the foregoing comments and amendments, reconsideration and allowance of all claims presently in the application are respectfully requested.

Applicants request any shortage of fees due in connection with the filing of this paper please be charged to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (case 501.37370CC4), and credit any excess payment of fees to such Deposit Account.

Respectfully submitted,

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